MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE
(UGC - AUTONOMOUS)

COURSE STRUCTURE
AND
DETAILED SYLLABI

MASTER OF TECHNOLOGY

VLSI & EMBEDDED SYSTEMS (VES)

M.Tech Regular Two Year P. G. Degree Course
(Applicable for the batches admitted from 2014-15)

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(An Autonomous Instititution, affiliated to JNTUA, Anantapur)

Course Structure and Syllabi

M.Tech. VLSI & Embedded Systems [VES]

I YEAR - I Semester

S. No	Course code	Subject	Theory	Lab.	Credits	I.M	E.M	M. M
1.	14VES11T01	VLSI Technology	4	0	4	40	60	100
2.	14VES11T02	Embedded System Concepts	4	0	4	40	60	100
3.	14VES11T03	Structured digital System design	4	0	4	40	60	100
4.	14VES11T04	Analog & Digital IC Design	4	0	4	40	60	100
5.	14VES11T05	Hardware Description Language	4	0	4	40	60	100
6.		Elective- I						
	14VES11E1a	1. MEMS			4	40	60	100
	14VES11E1b	2. RF IC Design						
	14VES11E1C	3. Device Modeling						
7	14VES11P01	Simulation and Synthesis Lab	0	3	2	40	60	100
		Contact periods/week	24	3				
		Total	27		26	280	420	700

I YEAR - II Semester

S.No	Course code	Subject	Theory	Lab.	Credits	I.M	E.M	M.M
1.	14VES12T06	Memory Technology	4	0	4	40	60	100
2	14VES12T07	FPGA Architectures & Applications	4	0	4	40	60	100
3	14VES12T08	Real Time Operating Systems	4	0	4	40	60	100
4.	14VES12T09	DSP Architecture and Applications	4	0	4	40	60	100
5.	14VES12T10	ASIC Design			4	40	60	100
6		Elective-II						
	14VES12E2a	1. Software Defined Radio	4	0	4	40	60	100
	14VES12E2b	2. Design & Testability						
	14VES12E2c	3. VLSI Signal Processing						
7	14VES12P02	FPGA Design Lab	0	3	2	40	60	100
		Contact periods/week	24	3				
		Total	27		26	280	420	700

II YEAR (III & IV Semesters)

S. No	Course code	Subject	Credits	I.M	E.M	M.M
1	14VES22S01	Seminar	2	50		
2	14VES22D01	Project work	16	40		

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M. Tech I Year - I Sem (VLSI & ES)

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4	0	4

VLSI TECHNOLOGY
(14VES11T01)

Course Objectives:

- To Study about the VLSI Technology properties.
- To provide Exposure about the different logical networks and sequential systems
- To Understand the VLSI Architecture Design and Floor Planning.
- To Learn CAD Algorithms and chip Designing Techniques.

Course Outcomes:

After Completion of this course students will be able to

- Understand the properties of Materials used in VLSI technology
- Represent and Realize their designs in Logical Networks and Sequential Systems
- Represent their designs of VLSI Architecture and Floor Planning.
- Understand concept of CAD algorithms and Chip Designing Techniques.

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids -Vds Relationships, Threshold Voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi-CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.
SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT IV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT V

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Text Books:

1. Essentials of VLSI Circuits and Systems, K. Eshraghianet . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf, Pearson Education, fifth Indian Reprint, 2005.

Reference Books:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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M. Tech I Year - I Sem (VLSI & ES)

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EMBEDDED SYSTEM CONCEPTS
(14VES11T02)

Course Objectives:

- To study about Concepts, Computing Platforms of Embedded Systems.
- To study about Architecture, Development tools of software and RTOS Concepts.

Course Outcomes:

After completion of this course students will be able to

- Know the Embedded System Concepts and its Computing Platforms and different interfacing techniques.
- Know the Architecture of Software.
- Know the Software Development Tools and RTOS Concepts.

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT IV

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

UNIT V

SYSTEM DESIGN TECHNIQUES:
Design methodologies, requirement analysis, specifications, system analysis and architecture design.
DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.
Text Books:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

Reference Books:

1. Embedded real time systems programming-sri ram V Iyer, pankajgupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002

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M. Tech I Year - I Sem (VLSI & ES)

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STRUCTURAL DIGITAL SYSTEM DESIGN
(14VES11T03)

Course Objectives:

- To study about structural functionality of different Digital blocks (Both combinational and Sequential)
- To provide an exposure to ASM charts, their notations and their realizations.
- To provide an exposure to VHDL and different styles of modelling using VHDL.
- To introduce concept of micro programming and study issues related to micro programming

Course Outcomes:

After Completion of this course students will be able to

- Understand structural functionality of different digital blocks
- Represent and Realize their designs in ASM charts
- Represent their designs in different modelling styles by using VHDL

Understand concept of Micro program and issues related to micro programming

UNIT-1

BUILDING BLOCKS FOR DIGITAL DESIGN: Multiplexer, Demultiplexer, Decoder, Encoder, Comparator, Adder, ALU, Carry-look-ahead adder.

BUILDING BLOCKS WITH MEMORY: Clocked building blocks, register building blocks, RAM, ROM, PLA, PAL, Timing devices.

UNIT -II

DESIGN METHODS: Elements of design style, top-down design, separation of controller and architecture, refining architecture, and control algorithm, Algorithmic State Machines, ASM chart notations.

UNIT-III

REALISING ASMS - Traditionalsynthesis from ASM chart, multiplexer controller method, one-shot method, ROM based method.

ASYNCHRONOUS INPUTS AND RACES - Asynchronous ASMs, Design for testability, test vectors, fault analysis tools.

UNIT-IV

MICROPROGRAM AND DESIGN: Microprogramming, Microprogramme sequencer 2910, designing microprogrammed computer. Power distribution noise, cross talk, reflections, line drivers and receivers.

UNIT-V

MODELLING WITH VHDL: CAD tools, simulators, schematic entry, synthesis from VHDL.

DESIGN CASE STUDIES: Single pulser, system clock, serial to parallel data conversion, traffic light controller.

Text Books:

1.Prosser and Winkel, "The Art of Digital Design", Prentice Hall.
2.Roth, “Digital System Design using VHDL”, Mc. Graw Hill, 2000

References:

1. William Fletcher, An Engineering Approach to Digital Design, 1st Edition, Prentice-Hall India, 1997.
2. William J Dally and John W Poulton, Digital Systems Engineering, Cambridge University Press, 2008.
3. JayaramBhasker, A VHDL Primer, 3rd edition, Prentice-Hall India, 2009.
4. J. Bhasker; A VHDL Primer, Addison-Wesley.
5. VHDL for Programmable Logic -Kevin Skahill, Cypress Semiconductors

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M. Tech I Year - I Sem (VLSI & ES)	**L**	**T**	**C**
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ANALOG & DIGITAL IC DESIGN
(14VES11T04)

Course Objectives:

- To understand basics of Integrated Devices and their Modelling.
- To learn about the mechanism of current mirrors and amplifiers.
- To understand various types of diversity and equalization techniques to current mirrors and operational amplifiers, Bi Cmos, Comparators.
- To Study about importance of oversampling convertors and Amplifiers
- To design and analyze Subsystem Process.

Course Outcomes*:*

After completion of this course the students will be able to

- Understand basics of Integrated Devices and Modelling.
- Know about the mechanism of Operational Amplifier and Compensation.
- Apply various types of diversity and equalization techniques to current mirrors and operational amplifiers, Bi Cmos, Comparators
- Recognize the importance of oversampling convertors and Amplifiers
- Analyze and design the subsystem processes.

UNIT I

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR

Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT. Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response

UNIT II

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION

Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation.

UNIT III

ADVANCED CURRENT MIRRORS AND OPAMPS

Advanced Current Mirror, Folded – Cascode Operational Amplifier, Current Mirror Operational Amplifier, Fully Differential Operational Amplifier. Common Mode Feedback Circuits, Current

Feedback Operational Amplifier, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

UNIT IV

OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling With and Without Noise Shaping. Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

UNIT V

SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-lookahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

Text Books:

1. BehzadRazavi, "Design of Analog CMOS Integrated Circuit" Tata-McGrawHill, 2002
2. D.A.JOHN & KEN MARTIN: "Analog Integrated Circuit Design". John Wiley, 1997.
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999

References:

1. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.
2. Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1997
3. Paul R.Gray.et.al, Analysis and Design of Analog Integrated circuits, John Wiley reprint, 4th edition, 2009.

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M. Tech I Year - I Sem (VLSI & ES)

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HARDWARE DESCRIPTION LANGUAGES
(14VES11T05**)**

Course Objectives:

- To study about Hardware Modelling, Switch level models with the VHDL.
- To study in detail about Behavioral Description, Data types and Operators in VHDL
- To study in detail about Synthesis of Combinational Logic Circuits

Course Outcomes:

- Students will be aware of different Modeling Systems using VHDL.
- Students will be able to get complete knowledge regarding Behavioral Descriptions, Data Types and Operators inVHDL.
- Students will be able to obtain the knowledge about Synthesis in VHDL.

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL:
User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL:
Verilog Behaviors, BehavioralStatements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks

and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT III

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic, Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT IV

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of UserDefined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT V

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

Text Books:

1.M.D.CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.

Reference Books:

1.M.G.ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.

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M. Tech I Year - I Sem (VLSI & ES)	**L**	**T**	**C**
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Elective I

MEMS
(14VES11E1a)

***Course Objective*:**

- Understanding of technology steps and technology process flows for MEMS components and systems.
- To understand the technologies for advanced MEMS.
- To get the knowledge of Technologies for system integration and different scaling issues.

Course Outcomes:

- Knowledge can be obtained by knowing the steps regarding the process flows of MEMS.
- To obtain the knowledge regarding advancement in MEMs.

UNIT I

INTRODUCTION: history of MEMS, market for MEMS, overview of MEMS processes properties of silicon, a sample MEMS process. Basics of Micro technology: definitions and terminology, a sample process, lithography and etching. MEMS Biosensors: Bio Flow Sensors, MEMS Images. Introduction to MEMS Pro design software.

UNIT II

MICROMACHINING: subtractive processes (wet and dry etching), additive processes (evaporation, sputtering, epitaxial growth). Fundamental Devices and Processes: basic mechanics and electrostatics for MEMS, parallel plate actuators, pull-in point, comb drives.

UNIT III

FUNDAMENTAL DEVICES AND PROCESSES: more electrostatic actuators; MEMS foundries, Cronos MUMPs (multi user MEMS process). MUMPs Multi User MEMS Process: JDS Uniphase MUMPs processing sequence and design rules. MUMPs and SUMMIT: design rules; applications; micro hinges and deployment actuators.

UNIT IV

CMOS MEMS: CMOS foundry processes, integrated IC/MEMS, MEMS post processing, applications.CLEAN ROOM LAB TECHNIQUES: clean rooms, gowning procedures; safety, fire, toxicity; acids and bases, photolithography.

UNIT V

MICROOPTOELECTROMECHANICAL SYSTEMS (MOEMS): micro scanners, digital mirror display, retinal scanning display. Grating light valve. Corner cube retroreflector, optical switches, other micro-optical devices applications.

Text Books:

1. HSU, TAI RAN, MEMS and Microsystems Design and Manufacture, Tata McGraw-Hill,2002.
2. Rai-Choudhury, Prosenjit; Mems and Moems Technology and Applications SPIE 2000.

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M. Tech I Year - I Sem (VLSI & ES)	**L**	**T**	**C**
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Elective I

RF IC DESIGN
(14VES11E1b)

Course Objectives:

- To provide knowledge about various basic concepts in RF design, Modulation and Detection Techniques.
- To know about methods of multiple Access Techniques, wireless standarads, Transceiver architectures.
- Estimate and detect the low-noise amplifiers & mixers, frequency synthesizers.

Course Outcomes:

The students will be able to apply various methods of signal estimation knowing the significance of each method.

- The students will be able to know RF design Modulation and Detection techniques.
- By applying suitable criterion the students will be able to learn about different wireless standarads, low-noise amplifiers & mixers.

UNIT I

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and Time Variance, Inter symbol Interference, Random Processes and Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation.

UNIT II

MODULATION AND DETECTION: General Considerations, Analog Modulation, DigitalModulation, Power Efficiency of Modulation Schemes, Noncoherent Detection.

MULTIPLE ACCESS TECHNIQUES AND WIRELESS STANDARDS: Mobile RF Communications, Multiple Access Techniques, Wireless Standards.

UNIT III

TRANSCEIVER ARCHITECTURES: General Considerations, Receiver Architectures, Transmitter Architectures, Transceiver Performance tests, Case Studies

UNIT IV

LOW-NOISE AMPLIFIERS AND MIXERS: Low-Noise Amplifiers, Down conversion mixers, Cascaded Stages Revisited. OSCILLATORS: General Considerations, Basic LC

Oscillator Topologies, Voltage-controlled Oscillators, Phase Noise, Bipolar and CMOS LC Oscillators, Monolithic Inductors, Resonator-less VCOs, Quadrature Signal Generation, Single-sideband Generation

UNIT V

FREQUENCY SYNTHESIZERS: General Considerations, Phase-Locked Loops, RF Synthesizer Architectures, Frequency Dividers.

POWER AMPLIFIERS: General Considerations, Classification of Power Amplifiers, HighEfficiency Power Amplifiers, Large-Signal Impedance Matching, Linearization Techniques, Design Examples.

Text books:

1. BehzadRazavi, "RF Micro Electronics", PHI publishers, 1998.
2. John Rogers, Calvin Plett, "Radio Frequency Integrated Circuit Design", Artech house Inc, London,
   2003.
3. Chris Bowick, "RF Circuit Design", Newness, Elsevier Science, 1982.
4. Willuam F. Egan, "Practical RF System Design", John Wiley & Sons, Inc., 2003.

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M. Tech I Year - I Sem (VLSI & ES)	**4**	**0**	**4**

Elective I

DEVICE MODELING
(14VES11E1c)

Course Objectives:

- To understand basic concepts of MOS, Characterstics, Techniques to measure high and low frequency, MOSFET parameters and Quantitative analysis.
- To analyze small scale analysis and Device applications.

Course Outcomes:

- After completing the course, the student will be familiar with basic concepts of MOS, Characterstics, Techniques to measure high and low frequency, MOSFET parameters and Quantitative analysis, small scale analysis and Device applications.

UNIT I

OVERVIEW of MOS: Characteristics of a MOS transistor-Surface properties of Silicon: Energy band diagram for the ideal case-Calculation of the threshold voltage (vt) – Non ideal effects- CV plots: importance – Ideal case – High frequency CV plots – low Frequency CV plots – Equations to CV plots – Deep depletion – Deviations from the Ideal CV plots: interface traps, Effect of AC signal on the interface states.

UNIT II

Techniques to measure Cit, computation of Cs and Ps – Limitation in high frequency techniques – Comparison of measurements at high and low frequency techniques. Sources of Oxide Trapped charge – radiation created oxide trapped charge – Experimental results – How Oxide Trapped charge can be annealed out – models to explain the technique – Shifts in threshold voltage in P-channel and N-channel MOSFET – Disadvantages – Shifts at dynamic bias – radiation hardening – Other alternatives dielectrics – gate metallization

UNIT III

MOSFET- Parameters of importance – Qualitative analysis of MOSFET – Mathematical model of IV characteristics – SPICE level1, level 2, level 3 models – Change in velocity with electric field – Expression for Id in the sub threshold region of operation. Non uniform doping and effect on threshold voltage – short channel effect – Narrow width effect – Small Geometry effects – Shrink and Scaling.

UNIT IV

Small signal analysis of MOSFET – Derivation of the different parameters associated with the small signal model – Cutoff frequency – Hot carrier effects – 1988 model – Monte-Carlo analysis. MOSFET devices – HMOS, DMOS, DIMOS, UMOS, VMOS, Sy MOSFET, SOS, Si MOX, BESOI, SEU, FAMOS, MCOS – Comparison with the conventional CMOS,MOS.

UNIT V

Device application: Depletion mode device – MOSFET connected as load devices - MOSFET as resistors, Static protection.

Text books:

1. Dewitt G. Ong, "Modern MOS technology: processes, Devices and Design", McGraw-Hill, 1984.
2. SorabK.Gandhi, "Semiconductor Device Principle", John Wiley & Sons, 1994.

Reference books:

1.Sze S.M., "VLSI technology", McGraw-Hill, 2003.
2.P Antognetti, G Massobrio, *Semiconductor device modelling with SPICE,* McGraw-Hill
3.P Ashburn, *Design and realization of bipolar transistors,* Wiley 1988.

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M. Tech I Year - I Sem (VLSI & ES)

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SIMULATION AND SYNTHESIS LAB
(14VES11P01)

Course Objectives:

- To study about Hardware Modelling, Switch level models with the verilog HDL.
- To study in detail about Behavioral Description, Data types and Operators in VHDL
- To study in detail about Synthesis of Combinational Logic Circuits.
- To study different methods of processing using MATLAB

Course Outcomes:

- Students will be aware of different Modeling Systems using VHDL.
- Students will be able to get complete knowledge regarding Behavioral Descriptions, Data Types and Operators inVHDL.
- Students will be able to obtain the knowledge about Synthesis in VHDL.

LIST OF EXPERIMENTS

1. Introduction to MATLAB Programming
2. Program assembly, Execution, Data processing and graphic analysis
3. Application of FFT for signal processing
4. Signal processing – Signal generation, filter design and analysis
5. MATLAB program to plot the one-dimensional rectangular potential well with infinite potential barrier
6. Numerical solution of the Schrodinger wave equation for rectangular potential well with infinite potential barrier using MATLAB program.
7. Design and simulation of (i) Combinational logic circuits, (ii) Sequential logic circuits, (iii) Analog circuits and (iv) A/D mixed circuits
8. Synthesis of Digital Circuit.
9. Place and Router Techniques for FPGAs.
10. Implementation of Design using FPGA and CPLD Devices.

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M. Tech I Year - II Sem (VLSI & ES)

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4	0	4

MEMORY TECHNOLOGY
(14VES12T06)

Course Objectives:

- To study about current technologies, integration methods and hardware and software design concepts associated with processor in Embedded Systems.
- To study about different types of memory and memory management schemes and various interfacing devices related to design of an Embedded System
- To get detail knowledge regarding testing and hardware software co- design issues pertaining to design of an Embedded System.

Course Outcomes:

After completion of this course the students will be able to understand

- Gets clear knowledge regarding current technologies and issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- Gets complete knowledge pertaining to different types of memory and memory management schemes and various interfacing devices related to design of an Embedded System.
- Different techniques related to testing and hardware software co- design issues pertaining to design of an Embedded System.

UNIT I

Introduction to Non-Volatile Memory: Introduction, Elementary memory concepts, Unique aspects of Non-volatile memory, Flash memory and flash cell variations, Semiconductor device Technology Generations.

UNIT II

Flash Memory Applications: Spectrum of memory devices, Evolving from EPROMs, Evolution of Flash usage models, Understanding flash attributes, Code storage, Data storage, Code and Data storage. Memory Circuit Technologies: Flash cell basic operation, Flash memory architecture, Redundancy, Error correction coding, Design of testability, Flash Specific circuit techniques.

UNIT III

NOR Flash stacked and Split-Gate Memory Technology: ETOX Flash cell Technology, SST Superflash EEPROM cell technology, Reliability issues and solutions, Applications. NAND Flash Memory Technology: Overview of NAND EEPROM, NAND Cell operation, NAND array

architecture and operation, Program threshold control and program V_t Spread reduction, Process and scaling issues, Key Circuits and Circuit technology interactions, Multilevel NAND.

UNIT IV

DINOR Flash Memory Technology: DINOR operation and array architecture, DINOR Technology features, DINOR Circuit for low voltage operation, Background operation function, P-Channel DINOR architecture. P-Channel Flash Memory Technology: Introduction, Device structure, Operations of P-Channel flash, Evolution of P-Channel flash.

UNIT V

Embedded Flash memory: Embedded Flash versus Stand alone flash memory, Embedded flash memory applications, Embedded flash memory cells, Embedded flash memory design.

Text Books:

1. J. Brewer and M. Gill, "Nonvolatile memory technologies with emphasis on Flash," IEEE press series on microelectronic systems, Wiley – Interscience, 2008.
2. T. Y. Tseng and S. M. Sze, "Nonvolatile Memories-Materials, Devices and Applications," American Scientific Publishers, Vol. 1 & 2, 2012.

Reference Books:

1.S. Lai, "Flash Memories: Successes and Challenges, IBM Journal of Res. & Dev. Vol. 52, p529, 2008.

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M. Tech I Year - II Sem (VLSI & ES)

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FPGA ARCHITECTURE & APPLICATIONS
(14VES12T07)

Course Objectives:

- To study about current technologies, integration methods and hardware and software design concepts associated with processor in Embedded Systems.
- To study about different types of programming logic devices and various interfacing devices related to FPGA design of an Embedded System
- To get detail knowledge regarding testing and hardware software co- design issues pertaining to design of FPGA architecture and applications.

Course Outcomes:

After completion of this course the students will be able to understand

- Gets clear knowledge regarding current technologies and issues relating to hardware and software design concepts associated with processor in FPGA.
- Gets complete knowledge pertaining to different types of programming logic devices and various interfacing devices related to FPGA design of an Embedded System.
- Different techniques related to testing and hardware software co- design issues pertaining to design of FPGA architecture and applications.

UNIT I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.

UNIT II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs. Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1, 2, 3 and their speed performance.

UNIT III

Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs, Problem of initial state assignment for one hot encoding. Derivations of state machine

charges. Realization of state machine charts with a PAL. Finite State Machines (FSM)-II Alternative realization for state machine chart using microprogramming. Linked state machines, One–Hot state machine, Petrinetes for state machines– basic concepts, properties, Extendedpetrinetes for parallel controllers. Finite State Machine–Case Study, Meta Stability, Synchronization.

UNIT IV

FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs, State machine designs centered around shift registers, One – Hot design method, Use of ASMs in One – Hot design. K Application of One – Hot method, System level design controller, data path and functional partition.

UNIT V

Digital front end Digital Design Tools for (FPGAs & ASICs) using Cadence EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs. Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Text Books:

1. P.K.Chan& S. Mourad, "Digital Design using Field Programmable Gate Array," Prentice Hall, 1994.
2. S.Trimberger, Edr., "Field Programmable Gate Array Technology," Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, "Field Programmable Gate Arrays," John Wiley & Sons, Newyork, Reprint 2008.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array," Kluwer Publications, 1992, 2nd Edition.

Reference Books:

1.Richard F Jinder , "Engineering Digital Design," 2nd Edition, Academic press.

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M. Tech I Year - II Sem (VLSI & ES)	**L**	**T**	**C**
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REAL TIME OPERATING SYSTEMS
(14VES12T08)

Course Objectives:

- To understand and review existing operating systems.
- To get complete knowledge regarding different interfacing techniques with respect to IEEE standaradsassocited with operating systems
- To get clear knowledge regarding classical Uniprocessor scheduling algorithms, Intertask communication & synchronization, Vx works.

Course Outcomes:

After completion of this course the students will be able to

- Gets review of Unix operating systems and its file systems & concepts.
- complete knowledge regarding different interfacing techniques with respect to IEEE standaradsassocited with operating systems.
- Understand basic concepts regarding to classical Uniprocessor scheduling algorithms, Intertask communication & synchronization, Vx works.

UNIT I

Brief Review of Unix Operating Systems: Unix Kernel – File system, Concepts of – Process, Concurrent Execution & Interrupts, Process Management – forks & execution, Programming with system calls, Process Scheduling, Shell programming and filters.

UNIT II

Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time Profile, POSIX versus traditional Unix signals, overheads and timing predictability. Hard versus Soft Real-time systems – examples, Jobs & Processors, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems.

UNIT III

Classical Uniprocessor Scheduling Algorithms – RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition. Concept of Embedded Operating Systems, Differences between Traditional OS and RTOS. Real-time System Concepts, RTOS Kernel & Issues in Multitasking – Task Assignment, Task Priorities, Scheduling.

UNIT IV

Intertask Communication & Synchronization – Definition of Context Switching, Foreground ISRs and Background Tasks, Critical Section – Reentrant Functions, Inter-process Communication (IPC) – IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

UNIT V

VxWorks – POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.Debugging Tools and Cross Development Environment – Software Logic Analyzers, ICEs, Comparison of RTOS – VxWorks, μC/OS-II and RT Linux for Embedded Applications.

Text Books:

1.Jane W. S. Liu, "Real Time Systems, Pearson Education," Asia, 2001.
2.Betcnhof, D.R., "Programming with POSIX threads," Addison - Wesley Longman, 1997.
3.C.M.Krishna and G.Shin, "Real Time Systems," McGraw-Hill, 1997.

Reference Books:

1.Jean.J.Labrosse, MicroC/OS-II, the CMP Books.
2.Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.

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M. Tech I Year - II Sem (VLSI & ES)

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DSP ARCHITECTURE AND APPLICATIONS
(14VES12T09)

Course Objectives:

- To study about the digital signal processing algorithms and multi rate signal processing
- To study about the architecture of TMS320CX processor, block diagram and syntax regarding assembly language.
- The study about the architecture, Data formats, Addressing modes, Advanced processors TMS320C54X.

Course Outcomes:

After completion of the course students will be able to

- Gets complete knowledge regarding various algorithms associated with Digital signal processing and multi rate signal processing.
- Verify the architecture of TMS320CX processor, block diagram and syntax regarding assembly language.
- Understand the about the architecture, Data formats, Addressing modes, Advanced processors TMS320C54X.

UNIT I

Fundamentals of Programmable DSPs: Multiplier and multiplier accumulator – Modified bus structures and Memory access in P-DSPs – Multiple access memory.

UNIT II

Multiport memory – VLIW architecture – Pipelining – Special addressing modes in P-DSPs – On chip peripherals.

UNIT III

TMS320C5X Processor: Architecture – Assembly language syntax – Addressing modes – Assembly language instructions – Pipeline structure, operation.
Block diagram of DSP (TMS320C5X) starter kit – Application programs for processing real time signals.

UNIT IV

TMS320C3X Processor: Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation.
Block diagram of DSP (TMS320C3X) starter kit – Application programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.

UNIT V

ADSP Processors: Architecture of ADSP-21XX and ADSP-210XX series of DSP processors – Addressing modes and assembly language instructions – Application programs – Filter design, FFT calculation.
Advanced Processors: Architecture of TMS320C54X: Pipeline operation, Code Composure studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors – Applications.

Text Books:

1. B.Venkataramani and M. Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications," Tata McGraw Hill, New Delhi, 2003.
2. User guides: Texas Instrumentation, Analog Devices, Motorola.

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M. Tech I Year - II Sem (VLSI & ES)

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ASIC DESIGN
(14VES12T10)

Course Objectives:

- To study ASIC types and library design with respect to design flow of CMOS transistors and design rules.
- To study in detail about sequential logic cells designed with transistors, programming ASIC logic cells.
- To study about Xilinx LCA, EPLD programmable ASIC design software.
- To study about logical synthesis and ASIC constructions.

Course Outcomes:

After completion of the course the student will be able to

- Gain complete knowledge regarding ASIC types and library design with respect to design flow of CMOS transistors and design rules.
- Gain complete knowledge regarding sequential logic cells designed with transistors, programming ASIC logic cells
- Know the Xilinx LCA, EPLD programmable ASIC design software
- Know about logical synthesis and ASIC constructions.

UNIT I

Introduction to ASICS, CMOS logic and ASIC library design: Types of ASICs – Design flow – CMOS transistors, CMOS design rules – Combinational logic cell.

UNIT II

Sequential logic cell – Data path logic cell – Transistors as resistors – Transistor parasitic capacitance – Logical effort – Library cell design – Library architecture. Programmable ASICs, Programmable ASIC logic cells and Programmable ASIC logic I/O cells: Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT.

UNIT III

Xilinx LCA – Altera FLEX – Altera MAX DC and AC inputs and ouputs – Clock and power inputs – Xilinx I/O blocks. Programmable ASIC interconnect, Programmable ASIC design software and low level design entry: Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX – Design systems.

UNIT IV

Logic Synthesis – Half gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.Logic Synthesis, Simulation and Testing: Verilog and logic synthesis – VHDL and logic synthesis – types of simulation – boundary scan test – fault simulation – automatic test pattern generation.

UNIT V

ASIC Construction, floor planning, placement and routing: System partition – FPGA partitioning – partitioning methods – floor planning – placement – Physical design flow – Global routing – Detailed routing – Special routing – Circuit extraction – DRC.

Text Books:

1.M. J. S. Smith, "Application Specific Integrated Circuits," Addition – Wesley Longman Inc., 1997.
2.FarzadNekoogar and FaranakNekoogar, " From ASICs to SOCs: A practical Approach," Prentice Hall PTR, 2003.
3.Wayne Wolf, "FPGA based System Design," Prentice Hall PTR, 2004.

Reference Books:

1.R. Rajsuman, "System - on – a – chip design and Test Santa Clara, CA," Artech House Publishers, 2000.
2.F. Nekoogar, "Timing Verification of Application Specific Integrated Circuits (ASICs)," Prentice Hall PTR, 1999.

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M. Tech I Year - II Sem (VLSI & ES)	**4**	**0**	**4**

Elective - II

SOFTWARE DEFINED RADIO (SDR)
(14VES12E2a)

Course Objectives:

- To study basic concepts of software radio, characteristics and designing principles of software radio
- To study in detail about radio frequency implementation issues, its dynamic rage, importance and overall performance.
- To study about Digital signal generation, smart antennas and their hardware implemtation.
- To study about object oriented representation of Radios and networks

Course Outcomes:

After completion of the course the student will be able to

- Gain complete knowledge regarding basic concepts of software radio, characteristics and designing principles of software radio.
- Gain complete knowledge regarding radio frequency implementation issues, its dynamic rage, importance and overall performance.
- Know about Digital signal generation, smart antennas and their hardware implemtation.
- Know about object oriented representation of Radios and networks.

UNIT I

Introduction to Software Radio Concepts: The need for Software radios and its definition, Characteristics and benefits of Software radio, Design principles of a software radio.

UNIT II

Radio Frequency Implementation Issues: Purpose of RF front – end, Dynamic range, RF receiver front – end topologies, Enhanced flexibility of the RF chain with software radios, Importance of the components to overall performance, Transmitter architectures and their issues, Noise and distortion in the RF chain, ADC & DAC distortion.
Pre-distortion, Flexible RF systems using micro-electromechanical systems, Multirate Signal Processing in SDR: Sample rate conversion principles, Polyphase filters, Digital filter banks, Timing recovery in digital receivers using multirate digital filters.

UNIT III

Digital Generation of Signals: Introduction, Comparison of direct digital synthesis with analog signal synthesis, Approaches to direct digital synthesis, Analysis of spurious signals, Spurious components due to periodic jitter, Bandpass signal generation, Performance of direct digital synthesis systems, Hybrid DDS – PLL Systems, Applications of direct digital synthesis, Generation of random sequences, ROM compression techniques.

UNIT IV

Smart Antennas: Introduction, Vector channel modelling, Benefits of smart antennas, Structures for beamforming systems, Smart antenna algorithms, Diversity and Space time adaptive signal processing, Algorithms for transmit STAP.
Hardware implementation of smart antennas, Array calibration, Digital Hardware Choices, Key hardware elements, DSP processors, FPGAs, Power measurement issues.

UNIT V

Object oriented Representation of Radios and Network: Networks, Object –oriented programming, Object brokers, Mobile application environments, Joint Tactical radio system.
Case Studies in Software Radio Design: SPEAKeasy, JTRS, Wireless Information transfer system, SDR-3000 digital transceiver subsystem, Spectrum Ware, Brief introduction to Cognitive Networking.

Text Books:

1. Jeffrey Hugh Reed, "Software Radio: A Modern Approach to Radio Engineering," Prentice Hall
   Professional, 2002.
2. Paul Burns, "Software Defined Radio for 3G," Artech House, 2002.

Reference Books:

1. Tony J Rouphael, "RF and DSP for SDR," Elsevier Newnes Press, 2008.
2. P. Kenington, "RF and Baseband Techniques for Software Defined Radio," Artech House, 2005.

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M. Tech I Year - II Sem (VLSI & ES)	**4**	**0**	**4**

Elective-II

DESIGN AND TESTABILITY
(14VES12E2b)

Course Objectives:

- To study different physical defects and their modeling, faults, test generation for combinational circuits.
- To study in detail about PLA testing, testing of sequential circuits and recent trends in VLSI testing

Course Outcomes:

After completion of the course the student will be able to

- Gain complete knowledge regarding different physical defects and their modeling, faults, test generation for combinational circuits.
- Gain complete knowledge regarding PLA testing, testing of sequential circuits and recent trends in VLSI testing

UNIT I

Physical defects and their modelling: Struck at faults, Bridging faults, Fault collapsing, Fault simulation: deductive, parallel and concurrent, critical path tracing.

UNIT II

Test generation for Combinational Circuits: D – Algorithm, Boolean difference, PODEM, and ATPG. Random, Exhaustive and Weighted: Random Test pattern generations, Aliasing and its effect on fault coverage.

UNIT III

PLA Testing: Cross point Fault model, Test generation. Memory Testing: Permanent intermittent and pattern sensitive faults, Delay faults and Hazards, Test generation techniques.

UNIT IV

Test generation for Sequential Circuits. Scan Design, Scan path and LSSD, BILBO, Concept of redundancy, spatial redundancy, Time redundancy.

UNIT V

Recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural Networks, Nano Scale Testing.

Text Books:

1. Stanley L. Hurst, "VLSI Testing: Digtal and mixed analogue digital techniques," Inspec/IEE, 1999.
2. LaungTerng Wang, Cheng Wen Wu, Xiaaqing Wen, "VLSI Test Principles and Architectures: Design and Testability."
3. Gordon Russell, "Advanced Simulation and Test Methodologies for VLSI Design."

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M. Tech I Year - II Sem (VLSI & ES)	**4**	**0**	**4**

Elective - II

VLSI SIGNAL PROCESSING
(14VES12E2c)

Course Objectives:

- To understand DSP systems and algorithms, properties, Fast convolution techniques
- To analyze tools regarding scaling and round off noise and numerical strength reduction.

Course Outcomes:

- After completing the course, the student will be familiar with the principles and the techniques used DSP systems and algorithms, properties, Fast convolution techniques, scaling and round off noise and numerical strength reduction.

UNIT I

Introduction To DSP Systems -Typical DSP algorithms - Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II

Retiming - definitions and properties - Unfolding – algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look-Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition. Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV

Scaling and round-off noise - scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined first-order filters.Bit-Level Arithmetic Architectures - parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon‟ s bit-serial multipliers using Horner‟ s rule, bitserial FIR filter, CSD representation, CSD multiplication using Horner‟ s rule for precision improvement.

UNIT V

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipeliningsynchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, twophase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol;Programming Digital Signal Processors – general architecture with important features, Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

Text Books:

1. KeshabK.Parhi, “VLSI Digital Signal Processing systems, Design and implementation,” Wiley, Inter Science, 1999.
2. Gary Yeap, “Practical Low Power Digital VLSI Design,” Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing,” McGraw-Hill, 1994.

Reference Books:

1. S.Y. Kung, H.J. White House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
2. Jose E. France, YannisTsividis, “Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing,” Prentice Hall, 1994.

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M. Tech I Year - II Sem (VLSI & ES)

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FPGA DESIGN LABORATORY
(14VES12P02)

Course Objectives:

- To synthesis and design using VHDL/ Verilog and mixed design and simulate using FPGA/CPLD blocks
- To implement on RTOS and experiments on Digital signal processors.

Course Outcomes: After completion of this course the students will be able to

- Gets Knowledge on synthesis and design using VHDL/ Verilog and mixed design and simulate using FPGA/CPLD blocks.
- Implemented and results on RTOS and experiments on Digital signal processors.

Note:

I. All the experiments are to be carried out independently by each student, with different specifications:

II. At least 15 experiments are to be carried out.

1. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after that Simulations are to be verified using FPGA/CPLD blocks from different commercially available products on:
   Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)
   Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.
2. Experiments on Digital Signal Processors.
3. Mini projects on RTOS